REMARKS

In the Official Action mailed on **May 26, 2004,** the examiner reviewed claims 1, 3, 4, 6-8, 10, 11, 13-15, 17, 18, 20, and 21. Claims 1, 3, 4, 6-8, 10, 11, 13-15, 17, 18, 20, and 21 were rejected under 35 U.S.C. §103(a) as being unpatentable over Greiner (USPub 2002/0157062, hereinafter "Greiner") in view of Rodriguez (USPub 2002/0087921, hereinafter "Rodriguez") and Carotti et al. (USPN 6,704,890, hereinafter "Carotti").

Rejections under 35 U.S.C. §103(a)

Independent claims 1, 8, and 15 were rejected as being unpatentable over Greiner in view of Rodriguez and Carotti. Applicant respectfully points out that Rodriguez teaches glitch detection circuitry on the strobe signal that can cause the system to **retry a transaction** when an error has occurred (see Rodriguez, paragraph [0025]).

In contrast, the present invention does not detect errors in the clock (strobe) signal. Instead, errors in any bit or in the clock signal are detected as errors in the reassembled data words **by the error detection and correction circuitry** (see FIGs. 4-5, and page 9, line 13 to page 10, line 16 of the instant application). The present invention operates by skewing the data in time prior to transmission, deskewing the data after reception, and using the error detection and correction circuitry to correct for any errors in the data bits or the clock. This technique is advantageous because even if multiple errors are caused by an erroneous clock signal, these errors appear as a single error across multiple words and can, therefore, be corrected by the error detection and correction circuitry. This facilitates correction of errors without retrying the transaction.

Additionally, Carotti teaches a serialiser/deserialiser that transmits data serially, **so that the clock signal can be recovered** from the data (see Carotti, FIG. 8 and col. 4, lines 28-36).

In contrast, the present invention regroups a plurality of data words so that bits from a given word are transmitted to the receiver in conjunction with bits from each of the plurality of data words (see Figs. 3B-C, and page 8, line 13 to page 9, line 10 of the instant application). This allows the present invention to use the error detection and correction circuitry to correct errors, even if the errors are caused by a faulty clock signal.

There is nothing within Greiner, Rodriguez, or Carotti, either separately or in concert, which suggests skewing the data in time prior to transmission, deskewing the data after reception, and using the error detection and correction circuitry to correct for any errors in the data bits or the clock, or to regroup the plurality of data words so that bits from a given word are transmitted to the receiver in conjunction with bits from each of the plurality of data words

Accordingly, Applicant has amended independent claims 1, 8, and 15 to clarify that the present invention skews the data in time prior to transmission, deskews the data after reception, and uses the error detection and correction circuitry to correct for any errors in the data bits or the clock. Additionally, Applicant has amended independent claims 1, 8, and 15 to clarify that the present invention regroups the plurality of data words so that bits from a given word are transmitted to the receiver in conjunction with bits from each of the plurality of data words. These amendments find support in FIGs. 3BC, 4, and 5, on page 8, line 13 to page 9, line 10, and on page 9, line 13 to page 10, line 16 of the instant application.

Hence, Applicant respectfully submits that independent claims 1, 8, and 15 as presently amended are in condition for allowance. Applicant also submits that claims 3-4 and 6-7, which depend upon claim 1, claims 10-11 and 13-14, which depend upon claim 8, and claims 17-18 and 20-21, which depend upon claim 15 are for the same reasons in condition for allowance and for reasons of the unique combinations recited in such claims.

CONCLUSION

It is submitted that the present application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

By _____
Edward J. Grundler
Registration No. 47, 615

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Edward J. Grundler
PARK, VAUGHAN & FLEMING LLP
508 Second Street, Suite 201
Davis, CA 95616-4692
Tel: (530) 759-1663
FAX: (530) 759-1665